WHAT IS CLAIMED IS:

1. A method for increasing a structure size of main structures in depth in a semiconductor substrate, comprising:

providing a semiconductor substrate comprising a crystalline material with a crystal lattice with crystal faces that are more resistant to etching and with crystal faces that are less resistant to etching;

arranging main structures on the semiconductor substrate in checkered fashion in a rectangular surface grid, at a surface of the semiconductor substrate, in each case in alternation with secondary structures formed in each case substantially in a section of the semiconductor substrate that is near a surface thereof;

setting x, y axes of the surface grid to be parallel to the crystal faces that are less resistant to etching; and

performing area-selective etching to increase the structure size of the main structures such that sections of the semiconductor substrate which are located below secondary structures are made available for the formation of extended main structures.

2. The method of claim 1, wherein a large structure having the main structures is imaged onto the surface of the semiconductor substrate by means of an exposure device with the x, y axes of the surface grid parallel to the crystal faces of the semiconductor substrate that are less resistant to etching.

3. The method of claim 2, wherein prior to imaging, a mask having a rectangularly patterned mask layout of the large structure is oriented in accordance with the crystal faces of the semiconductor substrate that are less resistant to etching.

4. The method of claim 1, wherein a semiconductor wafer is provided as the semiconductor substrate and a marking identifying a crystal orientation of the crystal lattice is provided at and/or on the semiconductor wafer.

5. The method of claim 4, wherein a crystal orientation identifying the orientation of the crystal faces that are less resistant to etching is identified by the marking.

6. The method of claim 5, wherein the marking is used for the orientation of a mask in an exposure device.

7. The method of claim 1, further comprising providing the main structures at the surface of the semiconductor substrate with an oval cross section.

8. The method of claim 1, wherein monocrystalline silicon is provided as the material of the semiconductor substrate.

9. The method of claim 8, wherein the surface grid is oriented in accordance with a <100> crystal orientation of the monocrystalline silicon.

10. The method of claim 9, wherein during the area-selective etching, the <100> crystal faces having a lower etching resistance are etched more rapidly than the <110> crystal faces that are more resistant to etching.

11. The method of claim 1, wherein the main structures, in upper sections between the surface of the semiconductor substrate and at least one lower edge of the secondary structures, are provided with a protective layer that is resistant at least toward the expanding etching process.

12. The method of claim 1, wherein the main structures are functionally designed as storage capacitances.

13. The method of claim 1, wherein the secondary structures are functionally designed as selection transistors assigned to the storage capacitances.

14. A semiconductor substrate structure, comprising:

a trench with a profile that is oval in plan view in an upper section adjoining the surface of the semiconductor substrate, with longitudinal sides parallel to the <100> crystal orientation, and with a profile that is essentially rectangular in a lower section below an etching-resistant protective layer, with longitudinal sides parallel to the <110> crystal orientation.

15. The structure of claim 14, wherein the protective layer extends up to a maximum of 1 micrometer below the surface of the semiconductor substrate.

16. The structure of claim 14, wherein the trench has, in the lower part, a bottle-like extension with a profile that is square in plan view and sides parallel to the <110> crystal orientation.

17. An arrangement of structures each consistent with the structure of claim 14, wherein the thickness of intermediate walls remaining between adjacent structures in the semiconductor substrate is of the order of magnitude of 100 nm.

18. The arrangement of claim 17, wherein the structures are designed as storage capacitances.

19. The arrangement of claim 17, wherein the structures comprise at least portions of DRAM cells.

20. The arrangement of claim 19, wherein the structures comprise storage capacitances.